SILVACO

Mobile Semiconductor

Using SmartSpice™ to Deliver Next-Generation, Low Power Memory Systems

The Customer

Mobile Semiconductor, a privately held U.S. company based in Seattle, Washington, is an independent memory compiler vendor specializing in Low Leakage / Low Voltage memory solutions. They also offer radiation-hardened embedded Memory IP to select markets. Mobile Semiconductor's catalog of over 60 memory compilers is targeted for a broad range of market segments, applications, and industries including A.I., machine learning, medical devices, smartphones, wearables, and IoT.

The Challenge

Mobile Semiconductor delivers memory compilers that rely on an accurate timing and power database to generate the right memory with the right performance. Memory characterization is needed to build this database and requires tens of thousands of SPICE simulations that can take weeks or even months to complete for all memory configurations.

Individual simulation runs are not trivial. The extracted post-layout simulation deck contains from 30K to 100K of transistors and at least three times that number of interconnect parasitic resistors and capacitors. Post-layout simulations with parasitics can be 10X longer that pre-layout analysis. Accuracy of analysis is essential to account for all the possible operating conditions of the memory, including process, voltage, and temperature corners.

Simulations can be a challenging for the numerical solvers used in SPICE software when complex circuits are analyzed in the latest advanced nanometer processes. Potential solver convergence issues for memory analysis can occur in timing loop, latch, and bitcell circuitry and require a stable and robust solver engine.

Statistical analysis of manufacturing effects on electrical behavior also must be analyzed to ensure the memories will have no yield issues. To achieve six-sigma reliability, thousand of simulations using Monte Carlo analysis and other statistical methods are required.

Key Challenges

Build a state-of-the-art memory characterization flow for the latest nanometer process technologies with:

- High accuracy
- Fast turn around time
- Reliable processing across various memory operating modes, foundry models, and compute servers

Silvaco Solution

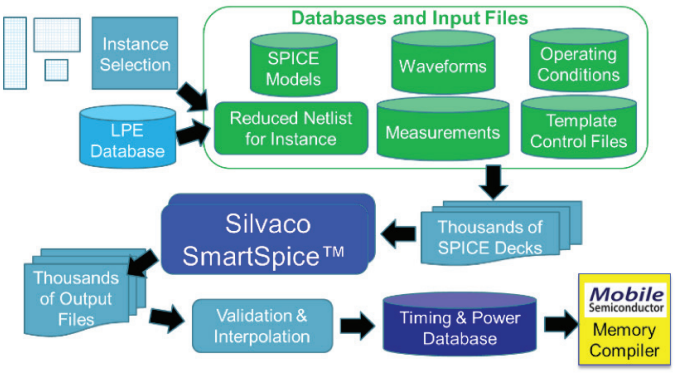
- SmartSpice circuit simulation with multi-CPU parallel processing, compatibility with other simulator formats, and high-accuracy standard foundry models
- SmartView waveform analyzer to consolidate and review all measurement from characterization runs

Results

- Market-leading simulation run time for 50,000 node post-layout circuits
- 50% faster throughput than legacy characterization flow
- High-accuracy of results including six-sigma variation analysis
- Renewed characterization

The Solution

Using Silvaco SmartSpice™, and help from Silvaco application engineers, Mobile Semiconductor created an automated memory characterization flow that delivered market-leading performance without sacrificing accuracy.



SmartSpice has the essential ingredients for successful memory characterization:

- Fast simulation times without sacrificing accuracy: Achieved the desired turnaround time to complete tens of thousands of simulation runs in days, not weeks, with the help of SmartSpice's advanced options and the assistance of Silvaco application engineers.
- Parallel processing that really works: Robust distribution of individual characterization runs across CPUs to analyze all PVT corners and statistical variations. SmartSpice seamlessly integrated in to Mobile Semiconductor's SQE queuing system for simulation runs.
- Reliable completion across hundreds of operating conditions and netlist variations: Robust convergence algorithms of SmartSpice handles all memory configurations and eliminates manual special-case handling.
- Consistent and predictable memory usage: Standard server configurations are sufficient for effective processing and does not require high-priced compute servers.
- Efficient Monte Carlo simulation times: Statistical analysis of potential manufacturing variations completed in a reasonable time.
- Control files and .measure statements compatibility: Control files from the legacy characterization flow did not require rewrite for easy adoption of Silvaco SmartSpice.
- Support of foundry device models: Foundry device models must be accurately implemented to achieve correct correlation with the PDKs of major foundries.

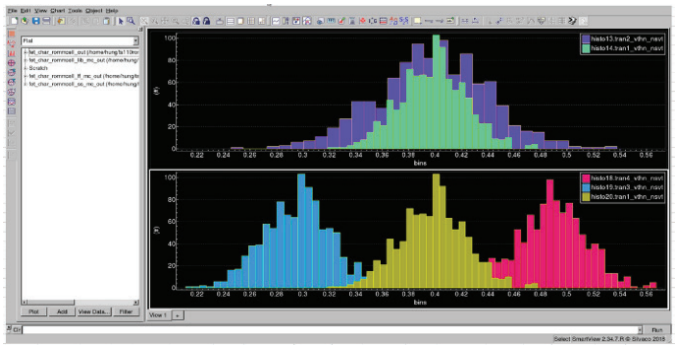
An example characterization of a 22nm SRAM instance illustrates the various measurements and tests that are done by SmartSpice to produce a Liberty file with over 200 parameters and 100 CCS constructs:

- 220 torture measurements to validate design
- 260 timing measurements
- 530 power measurements

Complete compiler characterization for the 22nm node requires 56,000 SPICE runs.

SmartView Waveform Debug

Thousands of simulations are run with hundreds of .measure statements to reveal circuit limitations and performance corners. The SmartView tool from Silvaco can combine, compare, and analyze these measurements and illustrate waveform behavior for detailed debug of any circuit.



Six sigma Monte Carlo analysis determines sensitivity of devices and combinations to parametric variations such as read current or write time.

True Cost of Simulation

Total simulation cost is more than the cost of software licenses. It is a product of CPU cost times software license cost plus engineering cost. Engineering cost depends on:

- Run time per analysis iteration, using as many CPUs as possible
- Difficulty of debug, requiring clear error messaging and easy waveform viewing

CPU cost (i.e. cloud pricing) is directly tied to:

- Memory required, less is better
- CPU count
- Wall clock run time

If the software licensing model is per CPU, the effect of adding multiple CPUs to the simulation flow is a net negative. A flexible simulation licensing model controls cost and removes simulation bottlenecks.

Mobile Semiconductor reduced the cost of its characterization environment and at the same time added more simulation licenses to take advantage of parallel processing.

Summary Results

Mobile Semiconductor improved characterization times by 50%, experienced an easy transition from a legacy simulator flow, and improved speed and quality of circuit debug with SmartSpice and SmartView. It found Silvaco's solution to be an excellent value in terms of easy integration, debug run time, and total cost of simulation combined with great support by Silvaco application engineers. Mobile Semiconductor will be using SmartSpice and SmartView for all future memory complier development.

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