AHB Octal SPI Controller with PSRAM and XIP Support

SILVACO

Overview

The Silvaco Octal SPI Memory Controller IP core is a serial peripheral interface (SPI) master which controls an external serial device, usually an industry-standard FLASH or PSRAM memory device.

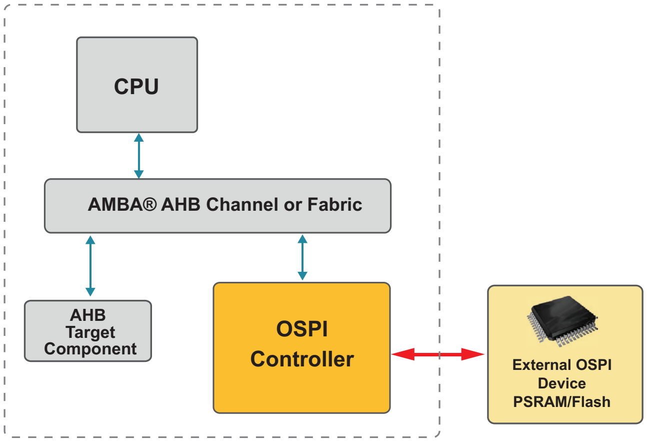
In Software Mode, an AHB Master may access the register interface of the Controller to implement a wide range of protocol variants and/or commands on the SPI bus. Programming options include transmission bit size, LSB/MSB first, SPI mode (the standard legacy 4-wire SPI bus interface or extended Dual, Quad or Octal Bus modes). Typical examples for software mode operations would be erasing and programming a FLASH device, or accessing the internal register set of a FLASH or PSRAM memory device.

The Execute in Place (XIP) Mode allows an AHB Master to directly read the contents of any of several industry-standard FLASH devices (such as Winbond, Macronix, Spansion and Micron devices) simply by reading from the address space of the OSPI Memory Controller.

The Bridge Mode allows an AHB Master to directly write to and read from the contents of any of several industry standard PSRAM devices (such as Infineon, APMemory). Supported standards for PSRAM devices include JEDEC JESD251A (Profile 2.0), HyperRAM and Xccela.

Features

- Compatible with industry-standard FLASH devices
- Compatible with PSRAM devices that conform to JEDEC JESD251A (Profile 2.0), HyperRAM, or Xccela standards
- Supports in-band slave reset signaling defined by JEDEC JESD252
- Software mode for direct control of registers
- Execute-in-place (XIP) mode for supporting direct reads from industry-standard FLASH devices
- Bridge mode for supporting direct writes and reads to/from industry standard PSRAM devices
- Automated command transmission support when entering/exiting XIP or Bridge modes
- AMBA AHB interfaces
- DMA Interface
- Interrupt control
- Configurable (16, 32, 64) word Transmit/Receive FIFOs
- Up to 4 slaves under Master control
- 4, 8, 16 or 32 bit serial transmit and receive
- Full duplex operation support
- Half duplex operation support
- DTR (Dual transfer rate) support
- Octal (I/O x 8) operation
- Quad (I/O x 4) operation



Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

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