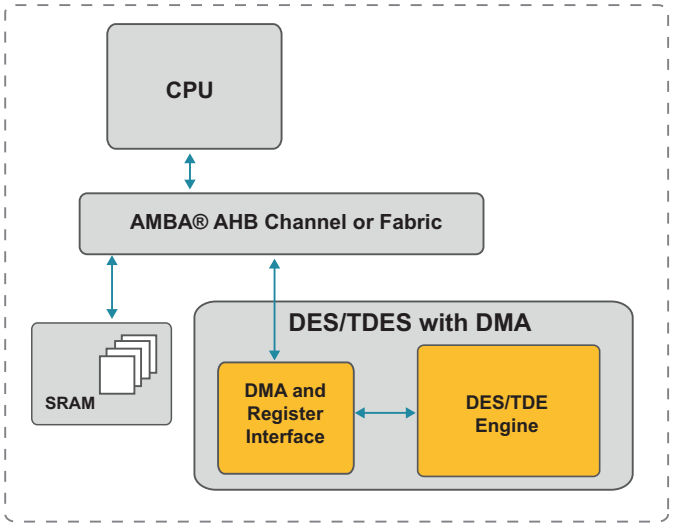
AHB DES and Triple DES with DMA

Overview

The AHB DES/TDES Encryption/Decryption Engine is a configurable core that interfaces to an AHB microprocessor bus. The Controller encrypts or decrypts blocks of data based on the DES encryption standard. In order to accommodate a wide variety of system requirements, the Engine can be generated in two modes: LowLatency and LowGateCount. For a TDES system, three DES cores are instantiated.

Features

- AHB Master component DMA
- AHB Slave component Register Interface
- DES/TDES modes supported:
- Electronic Code Book (ECB)
- Cipher Block Chaining (CBC)
- Output Feedback (OF)
- Maskable Interrupt



Deliverables

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

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