

AHB Low Power Subsystem - ARM Cortex M0

Overview

The AHB Low Power Subsystem is an AMBA® based system that is useful as the basic digital infrastructure for building low power SOCs. The subsystem contains a flexible Power Management Unit that controls the power sequence of the CPU as well as the APB peripherals. The PMU can easily be extended to control additional cores, peripherals and even mixed signal subsystems on the same SOC.

The AHB Low Power Subsystem includes a standard set of peripherals and cores that supports RTOS and software kernels. The package includes software for boot code, interrupt handlers and driver code.

The AHB Low Power Subsystem is soft IP that can be used in all the popular semiconductor technology nodes.

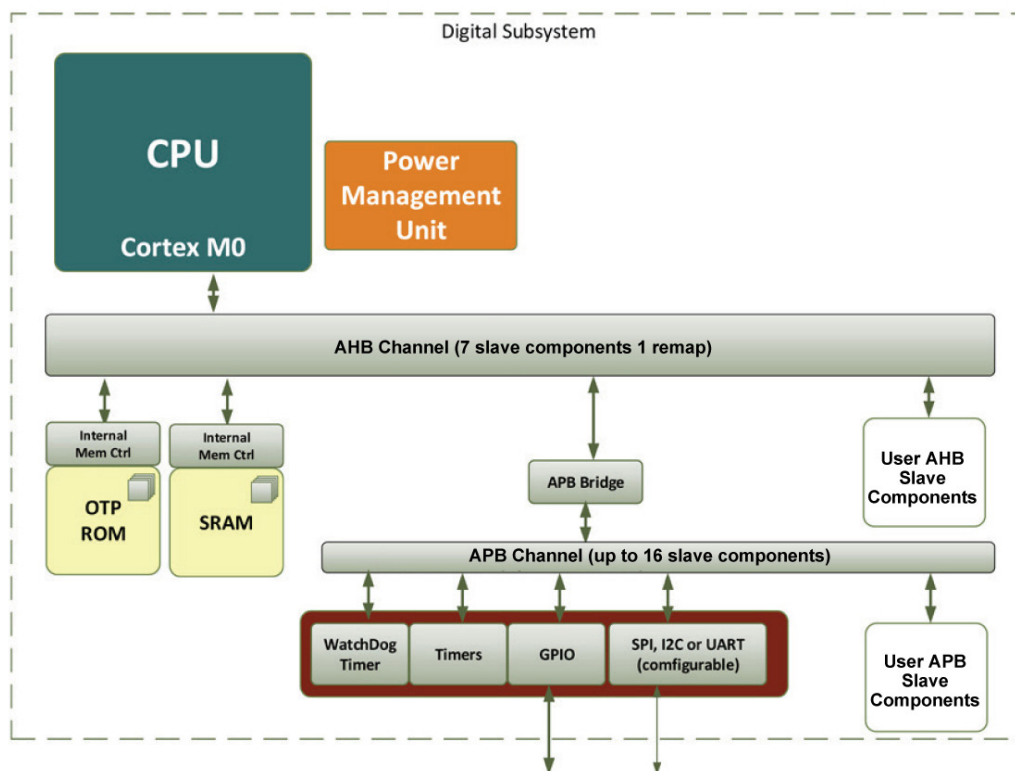
Features

- Low Power
- RTOS/Kernel Support
- AMBA AHB 2.0
- AMBA APB 3.0
- Power Management Unit
- Multiple Power Domains

Applications

- IoT Edge Devices
- Small Controllers
- Mixed Signal Digital - MEMS
- Smart Sensors
- Smart Lighting
- Health Monitors
- Power Management
- Industrial Sensors

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Processor Options

- ARM Cortex-M0

Infrastructure

- CPU
- AHB 2.0 Bus Channel / Decode
- APB 3.0 Bus Channel / Decode
- AHB to APB Bridge (2)

IP Cores

- Power Management Unit
- 8,16,32 bit Internal SRAM Controller
- Standard Peripherals
- Watchdog Timer, Timers (2), GPIO
- I2C Master/Slave components
- QSPI / SPI components
- 16550 UART
- Remap register
- Generic Registers

Software

- Startup and Interrupt code
- Example test code for all IP Cores
- Low power example project

Deliverables

- Verilog RTL source code
- Test bench with test suites
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints
- C software example projects