APB to AHB-Lite Asynchronous Bridge

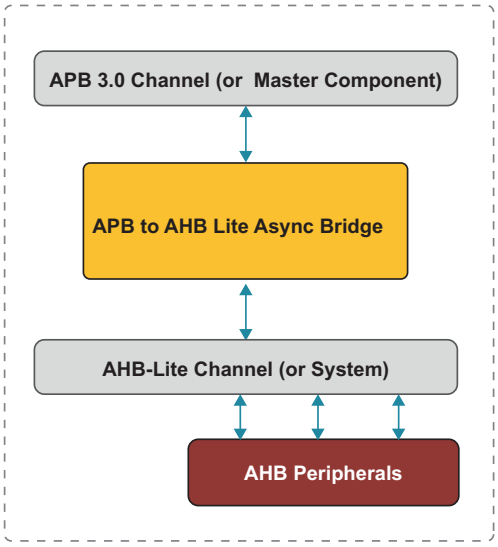
SILVACO

Overview

The APB to AHB-Lite Asynchronous Bridge translates an APB bus transaction (read or write) on one clock domain to an AHB-Lite bus transaction on a second (asynchronous) clock domain. This allows two completely independent AHB-Lite systems to communicate and share data. The bridge is implemented as two state machines - one on the initial or “A” domain and another on the secondary or “B” domain, and several synchronizers. The APB to AHB-Lite Asynchronous Bridge acts as an APB Slave component on the “A” domain, and an AHB-Lite Master component on the “B” domain.

Features

- Translates AMBA® APB transactions to AMBA® AHB-Lite transactions
- Interfaces two totally asynchronous APB and AHB-Lite domains
- Supports any ratio of relative clock frequencies
- Low Gate Count
- Conforms to APB and AHB-Lite signaling rules



Deliverables

- Verilog Source
- Complete Test Environment
- Bus Functional Model

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Rev 102424_04