Low Power Foundation IP

SILVACO

Overview

Silvaco's silicon proven Low Power Foundation IP includes Standard Cell libraries and Memory Compilers which enable designers to implement IoT designs for Always ON applications.

Our Low Power Foundation IP package provides Standard Cell libraries containing thousands of cells, and Single Port SRAM and ROM Memories. The Standard Cells and Memories are designed with extensive power saving techniques and the SRAM Memory contains extra low leakage modes to ensure the highest power savings at the required performance and area. Customers can use both the Standard Cells and Memories for designing industry leading low power chips in various technology nodes.

Applications

Memory

Silvaco's best in class Single Port SRAM is designed to achieve minimum power and area while meeting aggressive timing requirements.

This silicon proven memory utilizes a foundry bitcell with industry leading low Dynamic Power consumption, and multiple modes for extensive Static Power savings with low leakage.

Other features include Embedded Retention Switch options which provide flexibility and low power operation. It includes a Transition Ramp Controller (TRC) that enables control and a drastic reduction of the inrush current. Variable write mask and other standard optional features are also available.

Standard Cells

The Silvaco Low Power Standard Cell library provides highly optimized IP targeting low power and high-density applications.

Our solution delivers thousands of cells consisting of approximately 650 regular standard cells, more than 150 additional cells for low power and high speed and multiple gate length variants, with most available in five (5) VTs. They also come in twin / triple well options. This enables designs for applications from ultra-low power to high-speed.

The library is extended with a Power Management Kit, taking power reduction to the next level with features such as multi-voltage design and power gating.

Memory Features and Applications

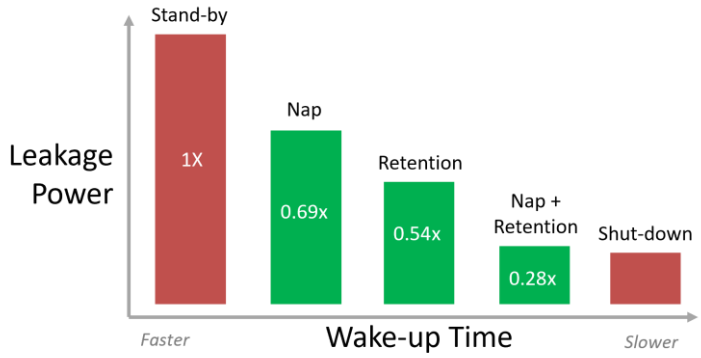
FEATURE	APPLICATION
Multiple Vt periphery	Architecture customized to provide better optimized target power, performance, area envelop
Embedded power switches	Saves SoC design time, area, and power while lowering risk
Segmented power control	Provides flexibility for segment power shut off and overall power management
Read and Write Assist	Low voltage and low power operation
Multiple power management modes	Offers multiple power saving customization options
Single power supply option	Easy integration

Standard Cell Features and Applications

FEATURE	APPLICATION
Multiple Vt and Well options	Customize designs for optimal low power performance and area implementation
Fine grained drive strengths and low leakage cells	Better low power implementation of designs
Power Management Kit	Enables power gating and multi voltage low power design methodologies
Multi-bit and multi-height standard cells	Better design implementation with sequential cells and MUX structures
ECO kit with fixed pattern for FEOL layers	Enables the flexibility of late layout modifications with minimal number of mask changes

Memory Power Management Modes

Multiple power modes for static power savings are available providing the flexibility to select the best trade-off between power saving and wake up time. Retention, retention-nap, and shut-down modes provide a progressive reduction of leakage power compared to stand-by mode.



Leakage data for 4Kx32 instance @ TT, 1.2V, 25°C

Standard Cells Low Power Strategies

The Silvaco Low Power Library enables the ability to combine multiple low power strategies to obtain compounded power savings.

- **Power gating** provides coarse grain block shut-down.
- **Level-shifters** enable multiple voltage domains, giving the flexibility of 1.2V and 0.9V operation for optimal performance at low power.
- **Low leakage cells** with long gate channel offer a low static power vs performance trade-off.
- **Fine grain drive** strengths provide more cell options during synthesis, reducing the usage of oversized cells.

Comprehensive Solution

Trusted Quality

- In volume production with multiple customer tapeouts
- Designed with high-sigma variation analysis to ensure high yield in manufacturing (global and local variation) using Silvaco's VarMan XMA variation analysis tool

Excellent Support

- Supports major EDA tool flows Custom PVT support
- Fast and efficient technical support

Silvaco Memory and Standard Cells are in volume production at multiple customers.
Silvaco offers a 30 day evaluation where customers can get access to Front End + LEF kit for PPA analysis. Contact a Silvaco representative for information.

For more information, please contact us at ip@silvaco.com.

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